REMARKS

Applicants appreciate the detailed examination evidenced by the Official Action mailed February 28, 2003 (hereinafter the "Official Action"). Applicants have amended independent Claims 1, 21, and 24 to further clarify the patentable subject matter recited therein. For example, independent Claim 1 has been amended to recited in part:

> implanting ions using the plurality of gate electrodes as an implant mask to form source/drain regions associated with the plurality of gate electrodes and **to define separate channel regions between adjacent isolation regions associated with the plurality of gate electrodes from the channel region** that are self-aligned to the plurality of gate electrodes.

Independent Claims 21 and 24 have been similarly amended.

As discussed in greater detail below, Odake does not disclose all the recitations of the amended independent claims. For example, the entire disclosure of Odake focuses on the formation of a single gate electrode (with a single associated channel region in the substrate) between isolation regions. Accordingly, the pending claims are patentable over the cited references for at least the reasons discussed herein.

Amended independent Claims 1, 21, and 24 are patentable over Odake.

Claims 1, 2, 3, 17. 21, 22, 23 and 24 stand rejected under 35 U.S.C. § 102(e) over U.S. Patent No. 6,165,825 to Odake ("Odake"). *Official Action, page 2.* Applicants have amended the indepdentn claims to further clairify the patentable duistianctions recited therein. For example, indepdent Claim 1 has been amednde to recite in-part:

> forming a mask on the isolation region that extends onto a portion of the substrate adjacent to the isolation region to provide a shielded portion of the substrate adjacent to the isolation region and an exposed portion of the substrate spaced apart from the isolation region having the shielded portion therebetween, the exposed portion of the substrate comprising a first portion where a gate electrode will be subsequently

formed and a second portion where a bit line contact will be subsequently formed, the mask exposing only the first and second portions;

implanting ions into the exposed portion of the substrate using the mask as an implant mask, thereby forming a channel region in only the first and second portions to adjust the threshold voltage of a transistor;

forming a plurality of gate electrodes on the channel region; and

implanting ions using the plurality of gate electrodes as an implant mask to form source/drain regions associated with the plurality of gate electrodes and to define separate channel regions **between adjacent isolation regions associated with the plurality of gate electrodes from the channel region** that are self-aligned to the plurality of gate electrodes.

As understood by Applicants, Odake discusses the formation of NMOS and PMOS transistors in a substrate. However, Odake does not disclose all the recitations of the amended independent claims. For example, Figures 5A – 5F of Odake (cited by the Official Action in support of the rejection) appear to show the formation of a single MOSFET with a single channel region beneath the gate electrode between each of the adjacent LOCOS layers 2. For example, Figure 5F of Odake shows four regions separated by LOCOS layers 2 each containing one of the gate electrodes 12 between adjacent LOCOS layers 2. Moreover, each of the single gate electrodes 12 has a single channel region there under in the substrate.

In contrast to Odake, the amended independent claims recite, for example, "implanting ions using the plurality of gate electrodes as an implant mask to form source/drain regions associated with the plurality of gate electrodes and **to define separate channel regions between adjacent isolation regions**." As demonstrated by the these emphasized portions of the recitations in the amended independent claims, separate channel regions are formed between adjacent isolation regions from a single channel region. For example, in some embodiments according to the present invention as discussed in reference to Figures 5 – 7 of the application, the channel region 122 is formed in the substrate 100 between adjacent isolation regions 102. Separate channel regions are formed between the adjacent isolation regions 102 by implanting ions to form the source/drain regions 142A/142B as shown, for example, in Figure 7. As discussed above, Odake discusses forming only a single channel region in the substrate between the LOCOS layers (as shown, for example, in Figure

5E) and implanting ions to form the source/drain regions 16 (as shown, for example, in Figure 5F of Odake). Accordingly, Odake does not disclose "implanting ions . . . **to define separate channel regions between adjacent isolation regions** associated with gate electrodes from the channel region as recited in the amended independent claims," as recited in amended independent Claims 1, 21, and 24.

Moreover, the passage of Odake cited by the Official Action in support of the rejection does not disclose defining separate channel regions from the channel region as alleged therein. The cited passage of Odake states that:

> In the step shown in FIG. 5(f), the reduction in thickness of the LOCOS layers 2 can be lightened in each of the MOSFET forming regions Rn1, Rn2, Rp2, Rp1. As a result, the ends of the LOCOS layer 2 are hardly removed owing to reduction in thickness as shown in a region Rx in FIG. 3. Accordingly, when high-concentration impurity ions are implanted for forming the source and drain regions, it is possible to prevent the source and the drain regions (N+ layers 16) from extending under the LOCOS layers 2 to generate junction leakage, as shown in a region Ry in FIG. 3. In particular, in a method using a salicide process, the portions in the vicinity of the surface of the source and drain regions are silicidized. During this process, if the ends of the LOCOS layers have been deeply removed, then the silicidation possibly proceeds under the LOCOS layers to generate short-circuiting electric current between adjacent MOSFETS. Also, the leakage between the source/drain regions and the substrate region is possibly increased. The semiconductor device of the second embodiment can effectively prevent such inconveniences.

Odake, column 12, lines 60 – 67 and column 13, lines 1 – 12.

As understood by Applicants, the above cited passage of Odake does not disclose implanting ions to "define separate channel regions between adjacent isolation regions from the channel region" as recited in the amended independent claims. In fact, the cited passage of Odake does not discuss channel regions at all.

Accordingly, amended independent Claims 1, 21, and 24 are patentable over Odake for at least the reasons discussed herein. Furthermore, dependent Claims 2 – 3, 17 – 20 and 23 are patentable at least per the patentability of amended independent Claims 1 and 21.

CONCLUSION

Applicants have amended the independent claims herein and have shown that the amended recitations are not disclosed by Odake. Accordingly, applicants respectfully request the withdrawal of all rejections and the allowance of all claims in due course. If any informal matters arise, the Examiner is encouraged to contact the undersigned by telephone at (919) 854.1400.

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CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: MS Non-Fee Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on May 22, 2003.

Audra Wooten
Date of Signature: May 22, 2003